AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions or listings of claims for this application.

Listing of Claims:

1. (Original) A memory device comprising:

a storage transistor at a surface of a substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, wherein the first and second source/drain regions are regions of a first conductivity type, and

a gate structure, wherein the gate structure wraps at least partially around the body portion in at least two spatial planes;

a bit line connected to the first source/drain region; and

a word line connected to the gate structure.

2. (Original) The memory device of claim 1, wherein the substrate is a silicon-on-insulator substrate.

3. (Original) The memory device of claim 1, wherein the storage transistor is a partially depleted device.

4. (Original) The memory device of claim 1, wherein the substrate is a semiconductor layer of a second conductivity type overlying a semiconductor layer of a first conductivity type.

5. (Original) The memory device of claim 1, wherein the storage transistor is a FinFET.

6. (Original) The memory device of claim 1, wherein the gate structure comprises a gate electrode, and wherein the gate electrode comprises a material from the group consisting of P+ polysilicon, N+ polysilicon, P+ Si_xGe_{1-x}, N+ Si_xGe_{1-x}, Ti, TaN, WN, and W.

7. (Original) The memory device of claim 1, wherein the gate structure comprises a metal gate electrode.

8. (Original) The memory device of claim 1, wherein the body portion contains a heavily doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region.

9. (Original) The memory device of claim 1, wherein the body portion contains an inert dopant region heavily doped with inert ions adjacent to the first source/drain region and separated from the second source/drain region.

10. (Currently amended) The memory device of claim 1, wherein the inert dopant region has a dopant dose within the range of approximately [[5e12]] $5x10^{12}$ atoms/cm^2 to approximately [[1e16]] $1x10^{16}$ atoms/cm^2.

11. (Original) The memory device of claim 1, wherein the storage transistor further comprises an insulating layer between the gate structure and the body portion, and wherein the thickness of the

insulating layer on a top surface of the body portion is greater than the thickness of the insulating layer on sidewalls of the body portion.

12. (Original) The memory device of claim 11, wherein the insulating layer is a material from the group consisting of silicon oxide, oxynitride, nitrided hafnium oxide, aluminum-doped hafnium oxide, hafnium oxide, aluminum oxide, zirconium oxide, tantalum pentoxide lanthanum oxide, titanium oxide, and yttrium oxide.

13. (Original) The memory device of claim 11, wherein the insulating layer is a material having a high dielectric constant.

14. (Original) The memory device of claim 1, wherein the storage transistor further comprises a higher Schottky barrier between the second source/drain region and the body portion than a Schottky barrier between the body portion and the first source/drain region.

15. (Original) The memory device of claim 14, wherein the storage transistor further comprises a silicide layer in contact with the second source/drain region.

16. (Original) The memory device of claim 15, wherein the storage transistor further comprises a silicide layer in contact with the first source/drain region.

17. (Original) The memory device of claim 1, wherein the first and second source/drain regions are raised such that the first and second source/drain regions share a same horizontal spatial plane as the portion of the gate structure on a sidewall of the body portion.

18. (Original) The memory device of claim 1, wherein the first and second source/drain regions each include a plurality of layers, and wherein the plurality of layers comprises at least one layer of a first material and at least one layer of a second material.

19. (Original) The memory device of claim 18, wherein the first and second materials have different band gaps.

20. (Original) The memory device of claim 18, wherein the plurality of layers are configured such that a first carrier type gains energy upon moving through the plurality of layers.

21. (Original) The memory device of claim 18, wherein the first and second materials have different valence band energies.

22. (Original) The memory device of claim 18, wherein the plurality of layers comprises alternating layers of Si_xGe_{1-x} and Si_yGe_{1-y}, respectively, where x is not equal to y.

23. (Original) A dynamic random access memory (DRAM) cell comprising:

a storage transistor at a surface of a silicon-on-insulator (SOI) substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, the body portion containing a heavily doped region of a first conductivity type adjacent to the second source/drain region and separated from the first source/drain region, the first and second source/drain regions being regions of a second conductivity type, and

a gate structure, the gate structure wrapping at least partially around the body portion in at least two spatial planes;

a bit line connected to the first source/drain region; and

a word line connected to the gate structure.

24. (Original) The DRAM cell of claim 23, wherein the body portion comprises at least one fin-shaped structure, wherein the storage transistor further comprises an oxide layer between the gate structure and the body portion, and wherein the thickness of the oxide layer on a top surface of each fin-shaped structure is greater than the thickness of the oxide layer on sidewalls of each fin-shaped structure.

25. (Original) The DRAM cell of claim 23, wherein the first and second source/drain regions are silicided differently from one another.

26. (Original) The memory device of claim 23, wherein the first and second source/drain regions have different dopant concentrations than one another.

27. (Original) The DRAM cell of claim 23, wherein the body portion comprises an inert dopant region adjacent to the first source/drain region, the inert dopant region having an amorphous dopant profile, and wherein the peak of the dopant profile is within a buried oxide layer.

28. (Original) A memory array comprising:

a plurality of memory cells, each memory cell comprising a storage transistor at a surface of a silicon-on-insulator (SOI) substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, the body portion containing a heavily doped region of a first conductivity type adjacent to the second source/drain region and separated from the first source/drain region, the first and second source/drain regions being regions of a second conductivity type, and

a plurality of gates at least partially surrounding the body portion;

a bit line connected to the first source/drain region; and

a word line connected to at least one gate.

29. (Original) The memory array of claim 28, wherein the plurality of gates are interconnected.

30. (Original) A semiconductor chip comprising:

a plurality of dynamic random access memory (DRAM) cells, at least one DRAM cell comprising a partially depleted storage transistor at a surface of a silicon-on-insulator (SOI) substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, the body portion comprising at least one fin-shaped structure and a region of a first conductivity type adjacent to the second source/drain region, the first and second source/drain regions being regions of a second conductivity type, and

a gate structure, the gate structure wrapping at least partially around each fin-shaped structure;

a bit line connected to the first source/drain region; and

a word line connected to the gate structure.

31. (Original) The semiconductor chip of claim 30, wherein the gate structure wraps uninterruptedly around three sides of each fin structure.

32. (Original) A processor system comprising:

a processor coupled to a memory device, the memory device comprising a plurality of memory cells, each memory cell comprising a storage transistor at a surface of a substrate, the storage transistor comprising:

a body portion between first and second source/drain regions, the first and second source/drain regions being regions of a first conductivity type, and

a gate structure, the gate structure wrapping at least partially around the body portion in at least two spatial planes;

a bit line connected to the first source/drain region; and

a word line connected to the gate structure.

33. (Original) The processor system of claim 32, wherein the substrate is a silicon-on-insulator substrate.

34. (Original) The processor system of claim 32, wherein the storage transistor is a FinFET.

35. (Original) The processor system of claim 32, wherein the body portion contains a heavily doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region.

36. (Original) The processor system of claim 32, wherein the body portion contains an inert dopant region heavily doped with inert ions adjacent to the first source/drain region and separated from the second source/drain region.

37. (Original) The processor system of claim 32, wherein the storage transistor further comprises an oxide layer between the gate structure and the body portion, and wherein the thickness of the oxide layer on a top surface of the body portion is greater than the thickness of the oxide layer on sidewalls of the body portion.

38. (Original) The processor system of claim 32, wherein the storage transistor further comprises a higher Schottky barrier between the

second source/drain region and the body portion than a Schottky barrier between the body portion and the first source/drain region.

39. (Original) The processor system of claim 38, wherein the storage transistor further comprises a silicide layer in contact with the second source/drain region.

40. (Original) The processor system of claim 39, wherein the storage transistor further comprises a silicide layer in contact with the first source/drain region.

41. (Original) The processor system of claim 32, wherein the first and second source/drain regions are raised such that the first and second source/drain regions share a same horizontal spatial plane as the portion of the gate structure on a sidewall of the body portion.

42. (Original) The processor system of claim 32, wherein the first and second source/drain regions each include a plurality of layers, and wherein the plurality of layers comprises at least one layer of a first material and at least one layer of a second material.

43. (Original) The processor system of claim 42, wherein the first and second materials have different band gaps.

44. (Original) The processor system of claim 42, wherein the plurality of layers are configured such that a first carrier type gains energy upon moving through the plurality of layers.

45. (Original) The processor system of claim 42, wherein the first and second materials have different valence band energies.

46. (Original) The processor system of claim 42, wherein the plurality of layers comprises alternating layers of Si_xGe_{1-x} and Si_yGe_{1-y}, respectively, where x is not equal to y.

47. (Original) A transistor device comprising:

a first source/drain region of a first conductivity type;

a second source/drain region of a first conductivity type;

a body portion for storing charge, the body portion protruding from a surface of a substrate, the body portion being located between the first and second source/drain regions, the body portion including a doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region; and

a gate structure wrapping around the body portion in at least two spatial planes.

48. (Original) The transistor device of claim 47, wherein the substrate is a silicon-on-insulator substrate.

49. (Original) The transistor device of claim 47, wherein the substrate is a semiconductor layer of a second conductivity type overlying a semiconductor layer of a first conductivity type.

50. (Original) The transistor device of claim 47, wherein the storage transistor is a FinFET.

51. (Original) The transistor device of claim 47, wherein the gate structure comprises a gate electrode, and wherein the gate electrode comprises a material from the group consisting of P+ polysilicon, N+ polysilicon, P+ Si_xGe_{1-x}, N+ Si_xGe_{1-x}, Ti, TaN, WN, and W.

52. (Original) The transistor device of claim 47, wherein the gate structure comprises a metal gate electrode.

53. (Currently amended) The transistor device of claim 47, wherein the region of a second conductivity type has an implant dose of between approximately [[5e12]] $\underline{5\text{x}10^{12}}$ atoms/cm^2 to approximately [[1e14]] $\underline{1\text{x}10^{14}}$ atoms/cm^2.

54. (Original) The transistor device of claim 47, wherein the body portion contains an inert dopant region heavily doped with inert ions adjacent to the first source/drain region and separated from the second source/drain region.

55. (Currently amended) The transistor device of claim 54, wherein the inert dopant region has a dopant dose within the range of approximately [[5e12]] $\underline{5\text{x}10^{12}}$ atoms/cm^2 to approximately [[1e16]] $\underline{1\text{x}10^{16}}$ atoms/cm^2.

56. (Original) The transistor device of claim 47, further comprising an insulating layer between the gate structure and the body portion, and wherein the thickness of the insulating layer on a top surface

of the body portion is greater than the thickness of the insulating layer on sidewalls of the body portion.

57. (Original) The transistor device of claim 56, wherein the insulating layer is a material from the group consisting of silicon oxide, oxynitride, nitrided hafnium oxide, aluminum-doped hafnium oxide, hafnium oxide, aluminum oxide, zirconium oxide, tantalum pentoxide lanthanum oxide, titanium oxide, and yttrium oxide.

58. (Original) The transistor device of claim 56, wherein the insulating layer is a material having a high dielectric constant.

59. (Original) The transistor device of claim 47, further comprising a higher Schottky barrier between the second source/drain region and the body portion than a Schottky barrier between the body portion and the first source/drain region.

60. (Original) The transistor device of claim 59, further comprising a silicide layer in contact with the second source/drain region.

61. (Original) The transistor device of claim 60, further comprising a silicide layer in contact with the first source/drain region.

62. (Original) The transistor device of claim 47, wherein the first and second source/drain regions are raised such that the first and second source/drain regions share a same horizontal spatial plane as the portion of the gate structure on a sidewall of the body portion.

63. (Original) The transistor device of claim 47, wherein the first and second source/drain regions each include a plurality of layers, and wherein the plurality of layers comprises at least one layer of a first material and at least one layer of a second material.

64. (Original) The transistor device of claim 63, wherein the first and second materials have different band gaps.

65. (Original) The transistor device of claim 63, wherein the plurality of layers are configured such that a first carrier type gains energy upon moving through the plurality of layers.

66. (Original) The transistor device of claim 63, wherein the first and second materials have different valence band energies.

67. (Original) The transistor device of claim 63, wherein the plurality of layers comprises alternating layers of Si_xGe_{1-x} and Si_yGe_{1-y}, respectively, where x is not equal to y.

Claims 68-110 (Canceled).